

High-Efficiency HBT MMIC Linear Power Amplifier for L-Band Personal Communications Systems

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Abstract—A heterojunction bipolar transistor (HBT) MMIC linear power amplifier is demonstrated for the 1.9 GHz Japanese Personal Handy Phone utilizing the $\pi/4$ DQPSK modulation technique. At an operating voltage of only 3 V, an output power of 21 dBm and a power added efficiency of 35% are obtained along with a modulation vector error of 4.5% and an adjacent channel interference of -60 dBc in ± 600 kHz offset frequency bands.

I. INTRODUCTION

IN TRANSMITTER applications of handsets for personal communications systems using the $\pi/4$ DQPSK modulation technique, both high linearity and high efficiency are desired. For the Japanese Personal Handy Phone (PHP) system, recently reported linear power amplifiers have provided an output power of 22 to 24 dBm at the 1-dB gain compression point (P1dB) with a power added efficiency (PAE) of 20 to 40% in single-tone CW operation at 1.9 GHz [1]–[5]. Although P1dB is a figure of linearity, a few dB backoff from P1dB is necessary, in order to meet the required specification for modulation vector error and adjacent channel interference. Thus, the efficiencies of these power amplifiers are generally reduced to 15 to 30%.

The objective of this work is to increase the efficiency of the MMIC power amplifier while operating with linearity well within the PHP specification. To this end a special circuit design, incorporating carbon-doped base AlGaAs/GaAs HBT's, was conceived. The low emitter-collector offset voltage and low resistances give a low saturation voltage, leading to efficient operation at 3 V.

II. CIRCUIT DESIGN

In CW operation, when the output power of a transistor biased in the linear region (class A or AB) is increased to the point where it begins to saturate (at around the 1-dB gain compression point), the phase of the output power deviates drastically. In the case of the $\pi/4$ DQPSK modulation signal, the phase deviation and power saturation drastically degrade the linearity of the transistor, since this modulation technique requires linearity of both phase and amplitude. Thus, to accomplish both high linearity and high efficiency simultaneously, increasing the output power whilst suppressing the phase deviation is crucial. Since the phase deviation can be attributed to the transistor entering the cutoff region and/or saturation region in its operating cycle, class A operation

would be effective in suppressing the phase deviation. In this work, therefore, the load lines, defined by the load impedance and bias condition, were determined so that HBT's could operate in fully class A.

The two-stage HBT MMIC linear power amplifier reported in this letter integrates three HBT's, all matching circuits and all bias circuits on a single chip. The HBT's are comprised of units with emitter finger length of 20 μm and finger width of 6.4 μm and are biased in the common emitter configuration. The dc current gain $\beta = 80$. Typical maximum available gain at a collector potential of 3 V and a collector current density of 10 kA/cm^2 is 21 dB at 1.9 GHz. Details of the HBT are described in [5], [6]. A four-unit HBT is used in the first stage for the rf amplification, and a four-unit and an 18-unit multiple emitter HBT are used in the second stage for the dc bias circuit and rf amplification, respectively. In the first stage, a combination of negative feedback and reactive matching is adopted for the reduction of phase deviation and for impedance matching. Negative feedback is also effective to ensure stable operation of the amplifier. In the second stage, reactive matching is adopted since the efficiency of the transistor in the second stage dominates the efficiency of the amplifier. The HBT MMIC linear power amplifier was designed using a nonlinear harmonic balance simulator with the Gummel-Poon model for the HBT's.

The fabricated MMIC chip is shown in Fig. 1. The chip size is 2.0 mm by 2.5 mm with a 200 μm thick GaAs substrate. The HBT MMIC amplifier, however, substantially occupies 2.0 mm by 1.5 mm, and the rest, 2.0 mm by 1.0 mm, is a 50 Ω coplanar waveguide transmission line. This results from the necessity of unifying chip size on the mask.

III. RF PERFORMANCE

Fig. 2 shows the 1.9 GHz CW test results of the fabricated HBT MMIC amplifier. The MMIC amplifier was biased at 3 V. A P1dB of 19.2 dBm and a PAE of 23% were obtained with a linear power gain of 25 dB and input VSWR of 1.8:1. Since a phase deviation of less than 1° was achieved for output power up to 22.7 dBm, suppression of the phase deviation was successfully realized.

Fig. 3(a) and (b) illustrates the measured performance with $\pi/4$ DQPSK modulation signals at 1.9 GHz. An output power of 21 dBm and a PAE of 35% were obtained along with a modulation vector error of 4.5% and an adjacent channel interference of -60 dBc in ± 600 kHz offset frequency bands. The input mean power of the modulation signal is 0.5 dBm, which is equal to the CW input power at the 2-dB

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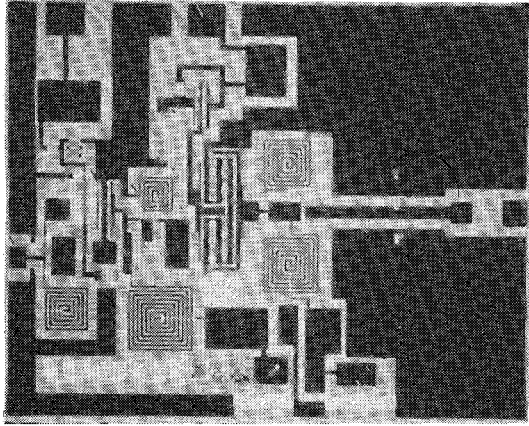


Fig. 1. Photograph of the HBT MMIC linear power amplifier.

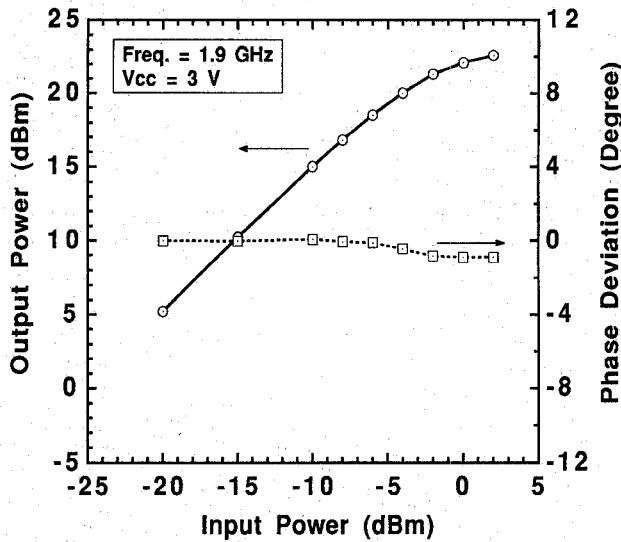
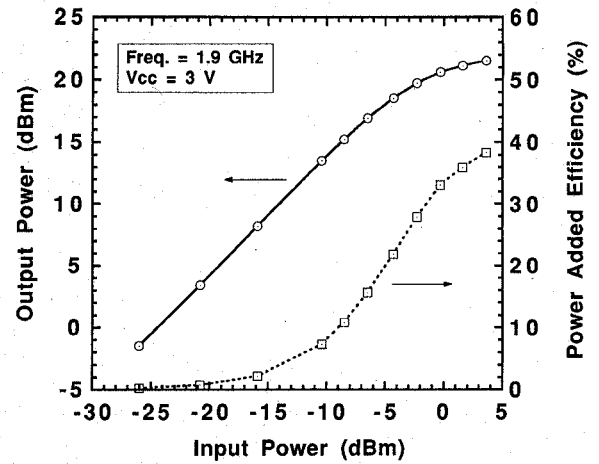


Fig. 2. Dependence of output power and phase deviation on input power in CW operation at 1.9 GHz.

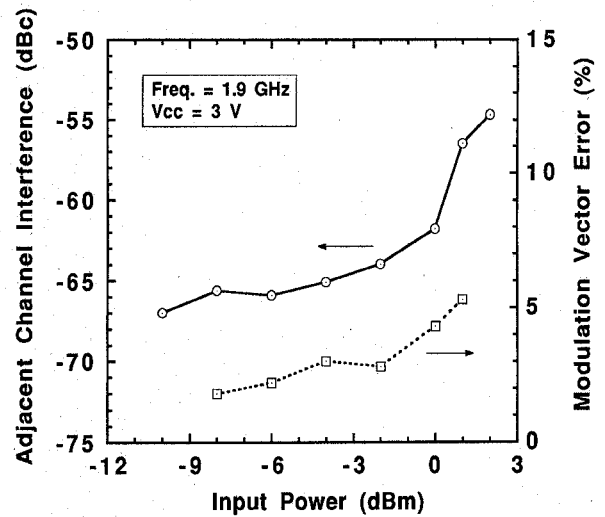
gain compression point (P2dB). Since the required linearity specification for the PHP system, related to the transmitter, is an adjacent channel interference of less than -50 dBc and a modulation vector error of less than 12.5%, the measured linearity is well within the specification.

Previously, we reported a two-stage HBT MMIC amplifier [5] which had excellent efficiency at low operating voltage. In that case, however, the linearity at P1dB did not meet the PHP system specification and a 3 dB output backoff from P1dB was necessary, causing a reduction in the PAE from 40% at P1dB to 25% at the 3 dB backoff point. The phase deviation at P1dB was about 6° . In the present work, the linearity at P2dB is much better than that required by the specification. Although the output power at P2dB is fairly distorted, the phase deviation is only 0.9° , as shown in Fig. 2. Thus, we believe that the high linearity in this work was accomplished due to the excellent phase linearity. This excellent linearity results in higher power amplifier efficiency.

In Fig. 4, the PAE and operating voltage of our amplifier are compared with those of previously reported results for PHP



(a)



(b)

Fig. 3. Performance of the HBT MMIC linear power amplifier with $\pi/4$ DQPSK modulation signal. (a) output power and power added efficiency, (b) adjacent channel interference in ± 600 kHz offset frequency bands and modulation vector error.

power amplifiers. In this Figure, the PAE is defined as the maximum PAE obtained when the linearity meets the system specification. The HBT MMIC power amplifier reported in this letter has exhibited excellent performance at an operating voltage of only 3 V.

IV. CONCLUSION

The fabricated HBT MMIC linear power amplifier exhibits a PAE as high as 35% with linearity well within the PHP specification, at an operating voltage of only 3 V. This work explicitly shows that suppressing the phase deviation is effective in improving the linearity under large-signal conditions. Moreover, the excellent linearity has led to higher MMIC power amplifier efficiency.

In PHP handsets, the power amplifier consumes a large fraction of the total dc power, and the battery size is limited by the operating voltage of the power amplifier. Thus, the operating

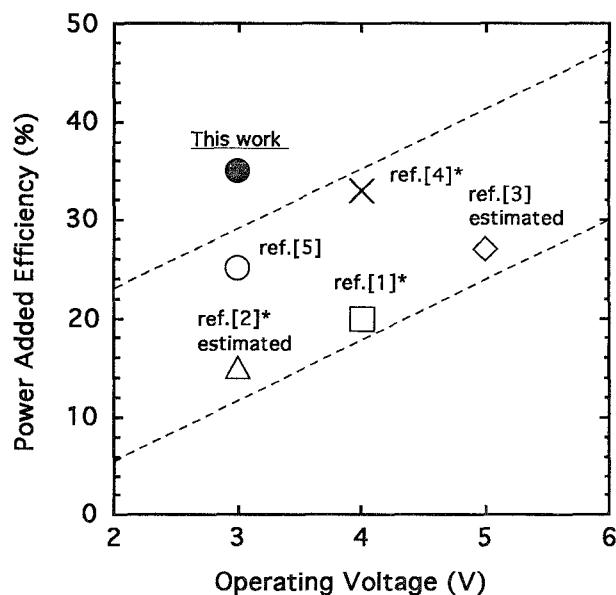


Fig. 4. Power added efficiency versus operating voltage of recently reported work. (*: the output matching circuit is off-chip.)

voltage and efficiency of the power amplifier dictate, to a considerable extent, the size, weight and maximum operating

time of the handset. The HBT MMIC power amplifier reported in this letter requires the battery to supply a dc current of only 120 mA at 3 V, allowing the PHP handset to have small size, light weight and long operating time.

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